Remarks

Claims 1, 2, 4, 6-10 and 12-16 are pending in the application. Claims 1, 2, 4, 9, 10 and 12-14 are allowed. Claims 6-8, 15 and 16 stand rejected. By this response, claims 6, 7, 10, 15 and 16 are amended. Applicants respectfully request that claims 1, 2, 4, 9, 10 and 12-14 be passed to issuance and that the Examiner reconsider pending claims 6-8 and 15-16.

Applicants' response to the instant office action is filed concurrently with a Petition to Withdraw Holding of Abandonment Under 37 C.F.R. 1.181(a) Based on Failure to Receive Office Action because Applicants never received the office action mailed on August 16, 2006. (see Applicants' attached Petition for Withdrawing Holding of Abandonment Under 37 CFR 181(a) Based on Failure to Receive Office Action.) Applicants have also filed concurrently herewith, a Request for Continued Examination of the instant application.

Claim Objections

The Examiner objected to claim 10 due the absence of a conjunctive "and" in line 5. Applicants have corrected this deficiency cited by the Examiner. Accordingly, the Examiner's objection has been overcome.

Claim Rejections - 35 U.S.C. § 102(e)

The Examiner rejected claims 6-8 under 35 U.S.C. § 102(e) as being anticipated by U.S Patent No. 6,414,868 to Wong, et al. The Examiner stated that Wong discloses a plurality of DRAMs capable of accepting non-inverted and inverted signals and a memory controlling capable of driving non-inverted and inverted signals to the DRAMs using a programmable pin, citing Figures 2, 3 and 5 corresponding to the limitations of Applicants' claimed memory system directed to the ability to accept non-inverting and inverting input as well as a memory controller capable of

driving either non-inverted or inverted signals to the DRAMs as configured with a programmable pin.

Applicants respectfully submit that Wong is directed to a memory expansion module incorporating control logic that facilitates switching from an upper bank of memory chips to a lower bank of memory chips. (Wong at Col. 2, lines 39-55; and Claim 1) Wong's bank control circuit 2000 facilitates communication with multiple memory banks without increasing the number of address inputs to the memory system. (Wong at Col. 1, lines 62-67 – Col. 2, line 1) In this regard, Wong's system enables memory expansion of a computer system using memory chips with the same capacity. (Wong at Col. 2, lines 34-38)

Wong discloses a memory system in which the RAS and CAS signals for multiple banks are selectable using conventional logic. The circuitry depicted in Figs. 2, 3 and 5 do not affect the polarity of the address or command signals presented to the memory. Instead, the non-inverted and inverted signals identified by the Examiner are used to control particular registers and assert specific RAS and CAS signals to control the selection of a particular memory bank. (Fig. 5 and Col. 5:10-20).

Conversely, Applicants' memory system "reduces the maximum count of drivers that will be switching in any one direction at a time, by utilizing a memory device that is designed to accept inverted inputs when so programmed." (Applicants' Specification at Paragraph 25) Applicants respectfully submit that Wong does not anticipate or suggest Applicants recited memory system because Wong is directed to a fundamentally different structure and function. Moreover, the use of inverting logic shown in Figure 5 of Wong represents the logic required to select a particular bank of memory rather than inverting some inputs and directing those inverted inputs to the memory. As such, Applicants respectfully submit that the memory system claimed herein is not anticipated or suggested by Wong.

The Examiner notes in the Remarks section of the Office action that Applicants' arguments distinguishing Wong "... are not germane to the claimed invention because the claim language

does not mention the particular type of limitations as noted by Applicant…" (p. 5 of Fin. O.A. dated 8/16/2006.) Accordingly, to more clearly define the subject matter of the invention herein, Applicants have amended claim 6 to recite a plurality of DRAMs "having receiver circuits adapted to interface with a plurality of signal drivers capable of providing both non-inverted and inverted address and command signal polarities to the plurality of DRAMs." Applicants have similarly amended claim 7 to recite that the memory controller "dynamically configures polarities of address and command signals exchanged between a plurality of signal drivers and the plurality of DRAMs."

Claim 7 as amended and claim 8 depend from claim 6 as amended. For the reasons noted above independent claim 10 as amended is allowable. Claims 12-14 depend from claim 10 as amended. Therefore, Applicants respectfully submit that the Examiner's rejection of claims 6-8, 10 and 12-14 under 35 U.S.C. § 102(e) has been overcome.

The Examiner rejected claims 15 and 16 under 35 U.S.C. § 102(e) as being anticipated by U.S Patent No. 6,414,868 to Wong, et al. The Examiner stated that Wong discloses a control circuit capable of conveying a plurality of inverted and non-inverted signals operable in the normal mode, such as accessing a memory data; and redrive circuitry which generates an output in both non-inverted and inverted polarity signals form one or more input signals. (1st OA at p. 6, citing Wong at Col. 1, lines 30-55) Applicants respectfully submit that the inverting and non-inverting control signals disclosed in Fig. 5 of Wong are exclusive to the bank selection logic of the bank control circuit 2000. That is, the inverting and non-inverting logic shown are not propagated to the memory address inputs but merely control which banks are selected.

The Examiner again stated that Applicants' arguments distinguishing Wong "are not germane to the claimed invention because the claim language does not mention the particular type of limitations as noted by Applicant…" Accordingly, Applicants have amended claim 15 to more clearly define the subject matter which Applicants regard as the invention to sharpen the distinction over the prior art to recite signal re-drive circuitry "adapted to invert an address or command input signal subsequently output to one or more of the plurality of DRAMs, wherein a

an output mode of the signal re-drive circuitry is responsive to a programmable input." Applicants have similarly amended claim 16 to recite re-drive circuitry "adapted to invert an address or command input signal subsequently output to one or more of the plurality of DRAMs via a programmable input, such that simultaneous switching noise is reduced."

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference. (MPEP §2131) Applicants respectfully submit that Wong does not teach or suggest Applicants' claimed memory system in which a memory controller responsive to a programmable pin directs selected banks of the memory to accept either a non-inverting or an inverting input to reduce simultaneous switching noise. (Applicants' Specification at Paragraph 22) Indeed, there is no teaching in Wong regarding modulating the logic polarity of selected memory bank inputs. Accordingly, Applicants respectfully submit that Wong does not anticipate the memory system claimed herein and that the Examiner's rejection of claims 15 and 16 under 35 U.S.C. § 102(e) has been overcome.

Allowable Subject Matter

Applicants gratefully acknowledge the Examiner's indication of allowed subject matter with respect to claims 1, 2, 4, 9, 10 and 12-14. Applicants have amended claim 10 to correct a grammatical deficiency and amended claims 6-8 and 15 and 16 to more clearly distinguish Applicants' claimed memory system over the prior art. Applicants respectfully submit that all pending claims are in condition for allowance.

Conclusion

Based on the foregoing, it is respectfully submitted the application may be passed to issuance.

The Examiner is urged to call the undersigned at the number listed below if, in the Examiner's opinion, such a phone conference would aid in furthering the prosecution of this application.

Respectfully submitted,
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